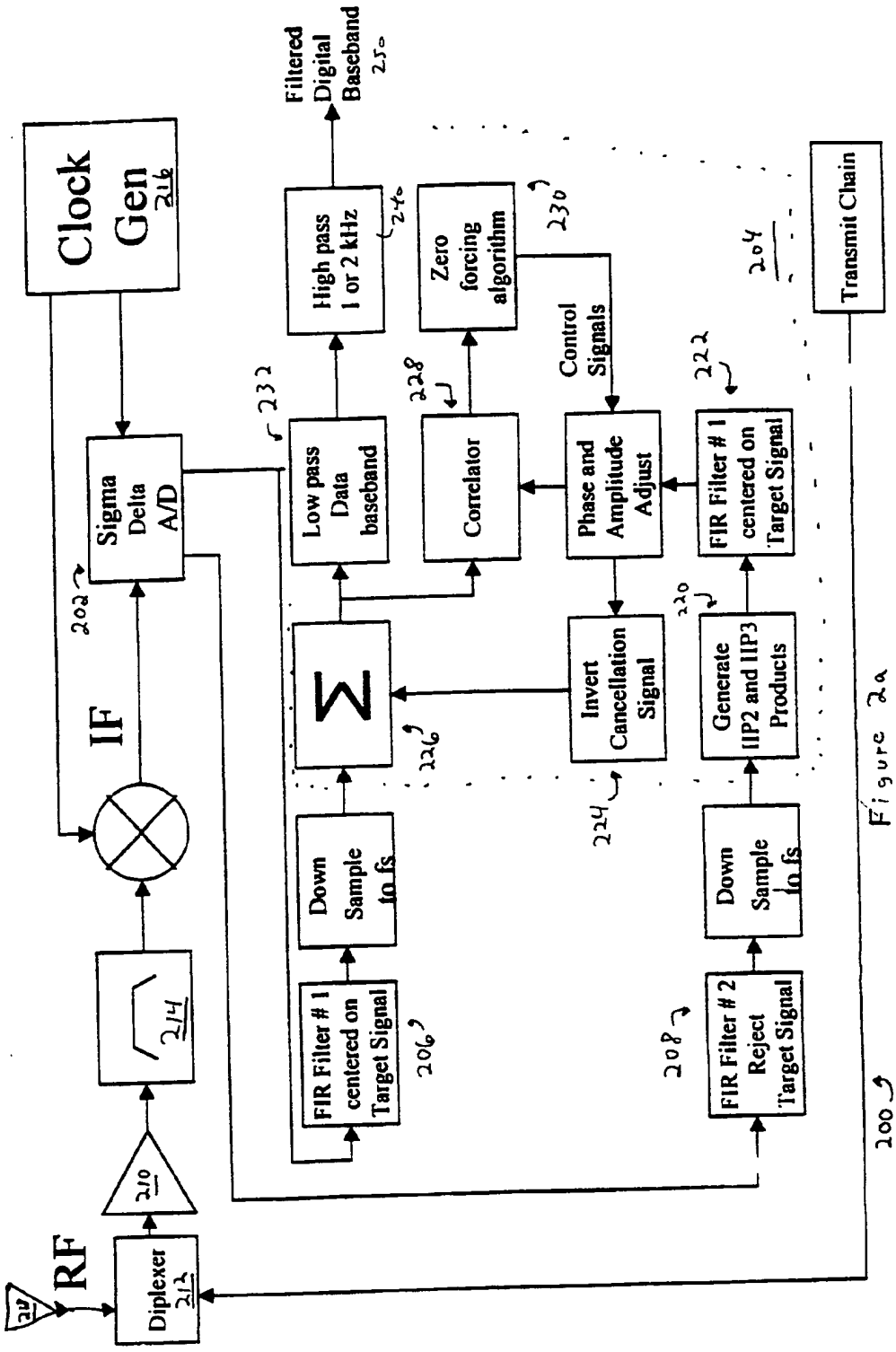



Figure 2a

[0075]
[0024, 0029]
CDMA
[0032, 0031]
[0132-0133]
CDMA Fig 7

Baseband processor base station?

Figure 3

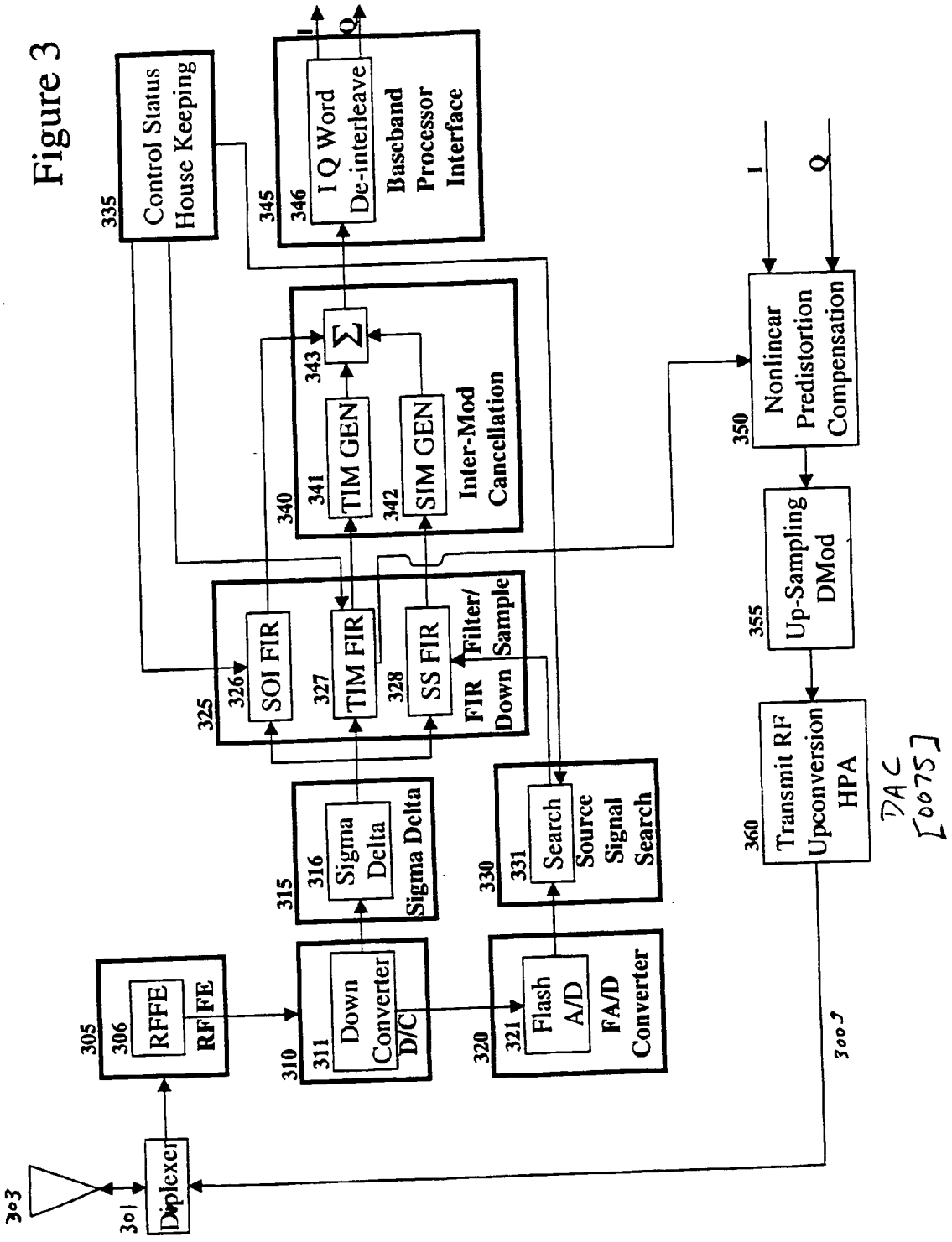
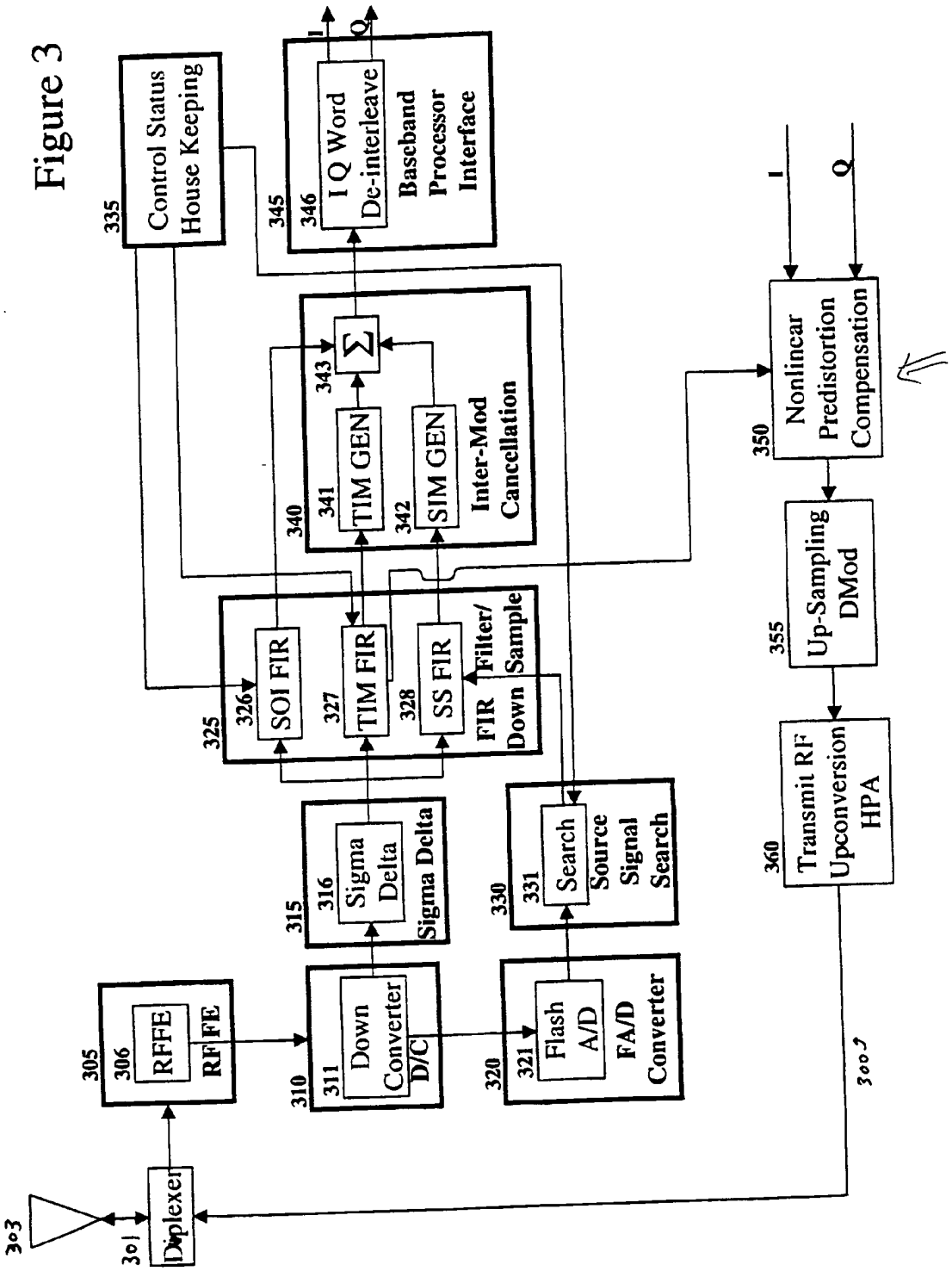

303
301
Diplexer
305
306
RFFE
RF FE
310
311
Down Converter
D/C
315
316
Sigma Delta
Sigma Delta
320
321
Flash A/D
FA/D Converter
330
331
Search
Source Signal Search
325
326
SOI FIR
327
TIM FIR
328
SS FIR
FIR Filter/ Down Sample
340
341
TIM GEN
342
SIM GEN
343
Σ
Inter-Mod Cancellation
335
Control Status House Keeping
345
346
I Q Word De-interleave
Baseband Processor Interface
I
Q
350
Nonlinear Predistortion Compensation
355
Up-Sampling DMod
360
Transmit RF Upconversion HPA
300
DAC [0075]

Figure 3


303
301
Diplexer
305
306
RFFE
RF FE
310
311
Down Converter
D/C
315
316
Sigma Delta
Sigma Delta
320
321
Flash A/D
FA/D Converter
325
326
SOI FIR
327
TIM FIR
328
SS FIR
FIR Filter/ Down Sample
330
331
Search
Source Signal Search
335
Control Status House Keeping
340
341
TIM GEN
342
SIM GEN
343
Σ
Inter-Mod Cancellation
345
346
I Q Word De-interleave
Baseband Processor Interface
I
Q
350
Nonlincar Predistortion Compensation
355
Up-Sampling DMod
360
Transmit RF Upconversion HPA
300

PGPUB-DOCUMENT-NUMBER: 20030021367

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030021367 A1

TITLE: Radio receiver

PUBLICATION-DATE: January 30, 2003

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APPL-NO: 10/ 146358

DATE FILED: May 14, 2002

RELATED-US-APPL-DATA:

non-provisional-of-provisional 60290781 20010515 US

non-provisional-of-provisional 60309602 20010803 US

non-provisional-of-provisional 60311942 20010813 US

non-provisional-of-provisional 60328125 20011009 US

INT-CL: [07], H03D001/04

US-CL-PUBLISHED: 375/346

US-CL-CURRENT: 375/346

REFERENCE-FIGURES: 2

ABSTRACT:

Various apparatuses and methods are described to reduce interference in signals subject to intermodulation products and high power narrow band interfering signals on lower power wideband signals. Apparatuses and methods described herein also provide the capability for supporting multi-standards, multi-modes and multi-bands in wireless and wired applications with a single receiver or a receiver with minor variations. The receiver described herein samples the entire band in which there can be signals of interest or signals that can generate interference. All of these signals are sampled in one bit stream and the bit stream is processed to isolate signals of interest and interfering signals. The isolated interfering signals are then cancelled out of the signals of interest.

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Detail Description Paragraph - DETX (26):
[0046] Decimating Filter--A filter associated with the Sigma Delta Modulator

or any digital down sampling filter. It provides narrow band filtering of the high speed, wide band, low resolution digital signal out of the sigma delta modulator and outputs a narrow band high resolution digital signal with many more bits of quantization. It may be a combination of multiple filters, but can be implemented as a **FIR filter**. It may be a multi-stage structure that filters and down samples in multiple steps. Decimating filters are used with conventional A/D converters, as well as sigma delta converters.

Detail Description Paragraph - DETX (29):

[0049] In general, various apparatuses and methods are described to reduce interference in a signal of interest that is going to be subsequently digitally down-converted. In an embodiment, a radio receiver includes a sampling rate multiplier coupled to one or more decimating filters (e.g., impulse response filters). In an embodiment in which a flash A/D converter is used instead of a sigma delta A/D converter, these filters are conventional digital **filters and may or may not be FIR filters**. The sampling rate multiplier samples a signal at an intermediate frequency (IF) that is to be demodulated at a sampling rate that is significantly greater than the sampling rate of a subsequent digital down conversion. The over sampling ratio will be between 10 and 100 normally. The filters associated with the sigma delta converter are rather complex and there may be a number of filters embodied in the decimating filters. The filters are decimating **filters (e.g., FIR filters)** that provide both the narrowband filtering and the down sampling functions. Each impulse response filter filters digitally a signal of interest and down-samples the signal at the second sampling rate in order to reduce interference in a signal of interest prior to the final digital down conversion. The decimating filters also increase the SNR in the narrow band signal by trading the wideband high sample rate for a narrow band lower sample rate at a greater number of bits of quantization.

Detail Description Paragraph - DETX (31):

[0051] FIG. 2A illustrates a block diagram of one embodiment of a radio receiver. Referring to FIG. 2A, the receiver 200 includes sampling rate multiplier 202, intermodulation compensator 204, a finite impulse response **(FIR) filter** 206 and a second FR filter 208, a low noise amplifier (LNA) 210, a duplexer 212, a surface acoustic wave (SAW) filter 214, and a clock generator 216. In one embodiment, clock generator function 216 is a dual function element in that it generates the mixing signal for a down conversion mixer and the sampling clock for sampling rate multiplier 202. In one embodiment, sampling rate multiplier 202 may comprise a Sigma Delta A/D converter or other similar device. A Sigma Delta A/D converter has a high bandwidth and samples at a rate greater than the final digital down conversion. The filtering and the down-sampling are done in the decimating filters of the sigma delta converter. The decimating **filters may be FIR filters** or a combination of digital filters. In the sigma delta terminology, the function is called the decimating filters. In an embodiment, **FIR filters** 206 and 208 comprise other filters such as decimating filters. In an embodiment, clock generator 216 is a local oscillator and generates the sampling clock for a sigma delta modulator. In one embodiment, a high bandwidth signal consists of a input frequency bandwidth of 60 to 140 megaherz or greater. The LO for down convertion to the IF is selected based on the RF band of interest (example around 1300 MHz for PSC band 1900 MHz down converted to 600 MHz IF). In one embodiment, the clock signal for the sigma delta A/D converter is at least 2.5 times the bandwidth of the fitler 214. For a band width of 120 MHz, the sampling rate is around 350 MHz. Two factors contribute greatly to determining the sigma delta sampling rate. First, the sampling rate is high enough to preclude aliasing and second.

the over sampling ratio (OSR) is high enough to yield adequate signal to noise ratio (SNR) after the decimating filters. The OSR is the ratio of the sigma delta 1 bit sampling rate to the nyquist sampling rate of the signal after the decimating filter. In one embodiment, the OSR is at least between 8 and 16 for 2.sup.nd or 3.sup.rd order sigma delta loop. This yields a SNR of around 40 dB, which, in turn, yields 6 bits of resolution.

Detail Description Paragraph - DETX (33):

[0053] In one embodiment, radio reciever 200 processes radio frequency (RF) signals received through antenna 218 with a convenient intermediate frequency. Receiver 200 samples the intermediate frequency with the low resolution (1 bit) sampling rate multiplier 202 and filters the digital samples with the one or more (decimating **filters) FIR filters** 206 and 208 as part of a subsequent digital down-conversion.

Detail Description Paragraph - DETX (35):

[0055] Radio receiver 200 has two parts: 1) sampling rate multiplier 202 coupled one or more **FIR filters** 206 and 208 and 2) intermodulation compensator 204. In the first part, radio receiver 200 significantly reduces the interfering signals and noise in the signal receive band via the RF SAW filter. Demodulation at an intermediate frequency (IF) via a sub-sampling technique (subsampling downconversion and decimation filtering) provides close-in rejection of unwanted signals. The IF analog waveform is sampled at a high rate relative to the bandwidth of the SOI and then the SOI is filtered by the decimating filter which then yields a narrowband signal with a high SNR and greater quantization from 1 bit to 6 or 8 bits. The harmonics of the sampling function are spaced a multiples of the sampling rate and thus a high sampling rate places the harmonics far apart. When the decimating filter performs the filtering on these harmonics, the tails from undesired harmonics and close in interfering signals are eliminated or greatly reduced. This steep filtering is possible in the digital domain, but is not as easily done in the analog domain. If the image filtering were performed after the down sampling as in a conventional A/D converter, the images would be closer together and there would be a greater aliasing problem. The steep filtering of close in signals would most likely still be achievable given sufficient quantization.

Detail Description Paragraph - DETX (36):

[0056] In one embodiment, sampling rate multiplexer 202 comprises a Sigma Delta analog to digital (A/D) converter that takes digital samples of the waveform at the IF. Each of **FIR filters** 206 and 208 filters the digital data samples from the Sigma Delta A/D converter prior to a subsequent (and first) digital down-conversion. In one embodiment, down-sampling the Sigma Delta samples occurs at, typically at least 4 to 8 times the symbol rate of this subsequent digital down-conversion. Since each of **FIR filters** 206 and 208 may be a fractionally spaced FIR, the band-shape around the desired signal can be controlled very accurately. In one embodiment, Sigma Delta A/D converter 202 samples at a rate 5 to 10 or more times the rate of the final digital down sampling rate and with an OSR of 10 to 20 or more. Thus, the sampling images are 5 to 10 times or more times farther apart in the frequency domain. Since each of **FIR filters** 206 and 208 filters at the Sigma Delta rate, the aliasing tails are significantly reduced when aliased into the baseband as a result of the final digital down-sampling. **FIR filters** 206 and 208 provide an "effective" sharp filter on the radio-frequency signal, and each harmonic, that assists in reducing close-in jamming signals. Aliasing tails from the harmonics appear as unwanted high-frequency signals and if not for **FIR filters**

206 and 208 could appear as undesired components in the digital signal after conversion into a digital value. In an embodiment, each **FIR filter** has programmable tap weights. The tap weights can be selected to compensate for either alpha band limiting or jammer rejection as described in more detail below. Alpha is the expansion over the Nyquist bandwidth i.e. 0.1 to 0.25 typically; this band limits the signal by introducing controlled inter-symbol interference.

Detail Description Paragraph - DETX (38):

[0058] In one embodiment, intermodulation compensator 204 receives two or more bit streams from Sigma Delta A/D converter 202 (based on the implementation and how many interfering signals are to be compensated), because Sigma Delta A/D converter 202 outputs two or more copies of the digital samples at a sampling rate greater than the sampling rate of the final digital down conversion. One output from Sigma Delta A/C converter 202 is sent to **FIR filter** 206, while the other copy is sent to **FIR filter** 208. **FIR filter** 206 operates as a band pass filter and filters one bit stream from Sigma Delta A/C converter 202 for the signal of interest, (such as the desired digital information signal at the IF), thereby producing the signal-of-interest that includes the in-band interference signal, but not the source signals if the interference signal was a product of intermodulation mixing. &p In one embodiment, **FIR filter** 208 operates as a band reject digital filter at the passband of interest for the signal of interest and produces a copy of the out-of-band signals that are the source of the in-band interference intermodulation products. The out-of-band signals are used to compute estimates of the in-band intermodulation products, which are then used to cancel the interference. A processor 220 computes the expected in-band interfering signals based on the IIP2, IIP3, and other attributes of the system such as phase and amplitude offsets.

Detail Description Paragraph - DETX (39):

[0059] **FIR filter** 222 is a band pass filter that passes the intermodulation products that fall in band of the SOI. The estimate of the interfering signal is inverted to produce a cancellation signal 224. An adder 226 adds the inverted cancellation signal 224 into the original desired signal from **FIR filter** 206 to cancel interference signals within the original Signal of Interest (SOI).

Detail Description Paragraph - DETX (42):

[0062] FIG. 2B illustrates a block diagram of a more detailed alternate embodiment of an intermodulation compensator. Referring to FIG. 2B, intermodulation compensator 204 operates similarly to the operation of the receiver in FIG. 2A described above. Intermodulation compensator 204 comprises a **FIR filter** and down sample cell that generates signals 206, 208A and 208B. In one embodiment, signal 206 is a 20 Mega sample per second, 6 bit signal of interest. Signals 208A and 208B represent the out of band signals are processed by processors 220A and 220B and they are also at 20 mega samples per second and 6 bits. Processor 220A and processor 220B are used to compute the estimate of the in band interference signals which will be used to cancel the interference signal inband of the SOI. Processor 220A and its associated components 224A and 228A phase adjust, amplitude adjust, and perform signal inversion on the computed transmitter feed through intermodulation products. Processor 220B and its associated components 224B and 228B phase adjust, amplitude adjust, and perform signal inversion on the computed intermodulation product from the source signals. The phase and amplitude adjusted inverted

signals from processors 220A and 220B are added to signal 206 via adder 226. The resulting signal is output to correlators 228A and 228B as well as I-Q de-interleaver and baseband processor interface cell.

Detail Description Paragraph - DETX (45):

[0065] Referring to FIG. 3, the receiver 300 includes a duplexer 301, an antenna 303, an RF front end cell 305, a down converter cell 310, a Sigma Delta cell 315, a flash A/D cell 320, a **FIR filter** and down sample cell 325 (also known a decimating filters), a search cell 330, a control and status/house-keeping cell 335, an intermodulation cancellation cell 340, a baseband processor interface 345. In the receiver, the Sigma Delta cell 315 and flash A/D cell 320 are sampling rate multipliers, but are used to two very different purposes. In the transmitter, there exists a non-linear pre-distortion compensation module 350, an up-sampling and delta modulator module 355, and a high power amplifier 360.

Detail Description Paragraph - DETX (46):

[0066] Antenna 303 is connected to duplexer 301. While in receiver mode, duplexer 301 feeds incoming signals into a RF front end (RFFE) cell 305. A RFFE module 306 in the cell receives the signal, amplifies the signal with a LNA, and filters the signal with a SAW filter. The amplified and filtered signal is passed to the IF down converter (D/C) cell 310. D/C cell 310 uses a down converter module 311 to down convert the signal. D/C cell 310 passes copies of the down converted analog signal to Sigma Delta cell 315 and flash A/D cell 320. Sigma Delta cell 325 uses a Sigma Delta A/D converter module 316 to produce multiple copies of samples of the signal to be sent to **FIR filter** and down sample cell 325 (decimating filters).

Detail Description Paragraph - DETX (47):

[0067] In one embodiment, **FIR filter** and down sample cell 325 contains three modules: a signal-of-interest **FIR module (decimating filter)** 326 to filter and down sample the signal-of-interest, a transmitter feed thru **FIR module (decimating filters)** 327 to filter and down sample the transmitter feed thru and the "half way signal", which is a signal half way between the transmit and receive band, and a source signal **FIR module (decimating filters)** 328 to filter and down sample other source signals. These signals are the signals in the receive band that create the intermodulation products that produce an interfering signal(s) in the SOI pass band. The transmitter feed thru path 327 can be used to cancel a close in jammer (close to the receive SOI) that can be modulated by the transmit signal feed thru. In one embodiment, the transmitter feed thru appears as a modulation on a high amplitude close-in blocking signal. The techniques described herein are intended to include the mitigation of this interference by the computation of the resultant interference in the band of the signal of interest. The blocking signal is isolated and it is used, along with the transmitter feed thru, to compute the estimate of the interference signal for cancellation of the inband interference.

Detail Description Paragraph - DETX (51):

[0071] All three of the filtered signals sets are passed from **FIR filter** and down sample cell (decimating filters associated with the sigma delta A/D) 325 to intermodulation cancellation cell 340. In intermodulation cancellation cell 340, a transmitter feed thru intermodulation products generation module 341 uses the filtered transmitter feed thru and associated interference source signal half way between the transmitter and the receiver signal to compute the

intermodulation interference produced by the transmitter feed thru and other mixing signal(s). A Source Signal Intermod (SIM) generation (SIM GEN) module 342 uses the filtered source signals from decimating filters 328 to compute the estimate of the intermodulation interfering signals. A cancellation summing cell 343 inverts and combines both of these signals with the filtered signal-of-interest to produce a signal-of-interest with the intermodulation interference canceled. The resulting signal-of-interest is sent to a baseband processor interface 345. In one embodiment, cancellation summing cell 340 includes a control loop that adjusts the phase and amplitude of the canceling signals to reduce, and potentially minimize, interference, as described in more detail below.

Detail Description Paragraph - DETX (55):

[0075] In one embodiment, the non-linear transmitter processor chain uses a similar architecture to transmit signals, a sigma delta D/A converter. In another embodiment, a conventional D/A converter with a conventional up conversion scheme may be used in conjunction with the non-linear pre-distortion. The I and Q digitally sampled signals are sent to a non-linear pre-distortion compensation module 350, which provides pre-distortion and combines the I and Q signals. In one embodiment, samples from the transmitter feed thru from the **receiver are used to update the pre-distortion** compensation. The update to the non-linear pre-distortion may be performed by comparing a copy of the transmitter feed thru signal (which is a copy of the transmitter signal after the high power amplifier (HPA) non-linearity) to a non-pre-distorted copy, or the original signal. If the non-linear pre-distortion in the transmitter has been done perfectly, the difference in these two signals is zero. Any variation indicates a need to update the non-linear pre-distortion corrections for the AM/AM and the AM/PM. In one embodiment, the copy of the transmitted signal is received from the receiver, and in another embodiment, the transmitter has a signal path used to down convert and demodulate a copy of the signal after it has gone thru the HPA. In either way, the non-distorted transmit signal is compared to the transmitted signal to update the pre-distortion function. This provides a continual update to the pre-distortion function over time and temperature which can be critical in devices without temperature compensation such as, for example, mobile devices. The combined signal is sent to up-sampling and delta modulator module 355 for up-sampling and delta modulation. Thereafter, the signal is up converted and amplified by transmit RF conversion and high power amplifier (HPA) 360. The amplified signal from HPA 360 is sent to duplexer 301 to be transmitted from antenna 303.

Detail Description Paragraph - DETX (63):

[0083] In one embodiment, BPF 410 is a programmable digital filter used to band pass the signal-of-interest and subsequently down sample to yield a high signal noise, narrow band, high bit resolution digital signal. In alternative embodiments, BPF filter 410 for the SOI is fixed and the LO is adjustable to place the signal of interest in the same place when the down conversion is performed. In one embodiment, this **filter is a FIR filter** with 90 to 128 taps. In another embodiment, the filter is a complex set of filters with intermediate down-sampling. In one embodiment, the **FIR filter** has programmable tap weights and the tap weights are selected for jammer rejection to reject jammer signals close to the signal-of-interest. In one embodiment, the jammer signals are as close as 900 kHz and 1700 kHz off center band of a 1.23 MHz wide signal. In alternative embodiments, the jammer source signals can be any where in the receive band. In one embodiment, the jammer signals are as high as -30 dBm with the signal-of-interest at -116 dBm. The output of BPF 410 is sent to

cancellation unit 428 (e.g., signal adder, summation unit, etc.) where the interference intermodulation product signals are cancelled.

Detail Description Paragraph - DETX (64):

[0084] In one embodiment, the intermodulation compensator 403 may operate as follows. BPF 412 band pass filters the transmit signal and any signal that falls "half way" between the transmitter and the receive signal. These half way signals, when mixed with the transmit feed through signal, can drop an intermodulation product in band of the signal-of-interest. Since the location of these signals is known, no search algorithm is required. In one embodiment, BPF 412 is a programmable **FIR filters** programmed to filter the transmitter signal and the other mixing signals. In alternative embodiments, BPF 412 may be a fixed set of filters. The output signals from BPF 412 are sent to a processing block 416 that generates an estimate of the intermodulation product(s). In one embodiment, these signals are 6 bits and 20 mega samples per second. The output of BPF 412 and the output of 410 are at the same quantization (number of bits) and clock rate. The source signals, and thus the estimate of the intermodulation products, are generated from the same bit stream as the SOI and this makes keeping the signals coherent much easier, which, in turn, makes generating accurate and timely interference cancellation signals possible. It is also easier to cancel the interference signals if all the signals have seen similar transfer functions.

Detail Description Paragraph - DETX (74):

[0094] In intermodulation cancellation signal generator 426 and intermodulation cancellation signal generator 432, the phase and amplitude of the estimate of the intermodulation product is adjusted with sufficient granularity so as to closely match the phase and amplitude of the intermodulation product generated in the non-linearities. When the number of samples is low relative to the carrier frequency, a simple delay of digital samples does not provide sufficient resolution of the phase adjustment. As an example, when the sample rate is 20 mega samples per second, and the IF is around 5 MHz (as can happen with the down sampling), each sample is only about 90 degrees. FIG. 11 shows how, in one embodiment, the phase is adjusted by any desired increment, even when the sample rate is low. In this embodiment, the original samples A, B, and C, are converted to samples a, b, c by weighted interpolation. The new samples a, b, and c are mapped into the time slots of A, B, C. In one embodiment, the phase shifting function is performed using a **FIR filter** with only a few taps. By properly selecting the weighting of values A, B, and C in the interpolation process, any arbitrary phase shift can be achieved. The amplitude may be adjusting by simple scaling.

Detail Description Paragraph - DETX (99):

[0119] In processing block 605, each copy of the signal is sent to a separate **FIR filter** in an intermodulation compensator. Note in alternative embodiments, there may be any number of copies of the signal processed to manage multiple intermodulation products. Each **FIR filter** filters its output signal at the Sigma Delta A/D converter sampling rate to reduce the interference from aliasing tails.

Detail Description Paragraph - DETX (100):

[0120] In processing block 610, one **FIR filter** operates as a band pass filter to pass the signal of interest at an intermediate frequency and produces the signal-of-interest with in-band interference (processing block 615).

Detail Description Paragraph - DETX (101):
[0121] In processing block 620, another **FIR filter** operates as a band reject filter for the signal of interest and produces out of band signals that are the source of the in-band interference intermodulation products.

Detail Description Paragraph - DETX (107):
[0127] In processing block 655, the intermodulation **compensator adjusts the phase** and/or amplitude of the estimated interference signals with a zero forcing (or other adaptive) algorithm and generates a signal to control generation of the invert cancellation signal. The control loop may run continuously to adaptively cancel the in-band interfering signals.

Claims Text - CLTX (54):
53. The method defined in claim 52 wherein the first and second decimating **filters comprise FIR filters**.

Claims Text - CLTX (55):
54. The method defined in claim 53 wherein the first and second **FIR filters are fractionally spaced FIR filters**.

Claims Text - CLTX (57):
56. The method defined in claim 52 wherein the first and second **FIR filters** are applied at a rate at which the Sigma Delta A/D converter is applied.

Claims Text - CLTX (71):
70. The apparatus of claim 69, wherein at least one of the impulse response filters comprises a finite impulse response **(FIR) filter**.

Claims Text - CLTX (73):
72. The apparatus of claim 70, wherein at least one of the **FIR filters** has programmable tap weights selected to cause filtering for jammer rejection.

Claims Text - CLTX (76):
75. The apparatus of claim 73, wherein the intermodulation **compensator phase** adjusts the estimations of interfering intermodulation signals to reduce interference in the sampled digital data samples.

Claims Text - CLTX (85):
84. The apparatus of claim 83 wherein at least one decimating **filter comprises at least one FIR filter**.

Claims Text - CLTX (86):
85. The apparatus of claim 83, wherein the **FIR filter is a fractionally spaced FIR filter**.

Claims Text - CLTX (87):

86. The apparatus of claim 83, wherein spacing in the **FIR filter** is programmable.

Claims Text - CLTX (95):

94. The apparatus of claim 91, wherein the intermodulation **compensator phase** adjusts estimations of interfering intermodulation signals and adds the phase adjusted estimations to the signal of interest to reduce interference in the sampled digital data samples.